AMENDMENTS IN THE SPECIFICATION:

Please replace the paragraph beginning on page 3, line 30 and ending on page 4, line 19, with the following amended paragraph:

Fig. 12 shows a construction of the inverter 101 comprising a PMOS transistor and an NMOS transistor. In a rising transition at the output terminal Y, as the potential at the input terminal A goes from ~~a low level (L) to a high level (H)~~ a high level (H) to a low level (L), the PMOS transistor P1 makes a transition from an OFF state to an ON state so as to charge an output load. When ~~an increase~~ a decrease in the potential between the source and drain of the PMOS transistor P1 is relatively ~~smaller~~ bigger than the magnitude of change in the gate potential, a transition from a region, characterized by an increase in a current with time, to another region characterized by a rapid exponential decrease in the current occurs (see pattern 2 of Fig. 5). Referring to Fig. 13, in the related-art source model 106, an internal voltage source E(t), whose voltage level shows a linear variation between 0 [[ad]] and Vdd in a time Δt, is used to represent the transition described above.